MULTIMEDIA UNIVERSITY

STUDENT ID NO

Table No.	

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 1, 2022/2023 (TERM ID 2210)

PDS0101 – INTRODUCTION TO DIGITAL SYSTEMS

(All sections / Groups)

15 FEBRUARY 2023
2:30 PM – 4:30 PM
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 11 pages including cover page with 5 Questions. Attempt **ALL** questions.
2. The total mark for this paper is 50 marks.
3. Write all your answers in this booklet.

QUESTION 1

a) Machine A is having frequency of 100Hz. [4 marks]

i. Explain what does it mean by frequency of 100Hz ?
ii. What is the time needed to transmit 1 bit of data?
iii. What is the time needed to transmit 1B of data serially?
iv. What is the time needed to transmit 1B of data in parallel?

b) Convert 246.7_8 to the following number systems. Show all steps. [3 Marks]

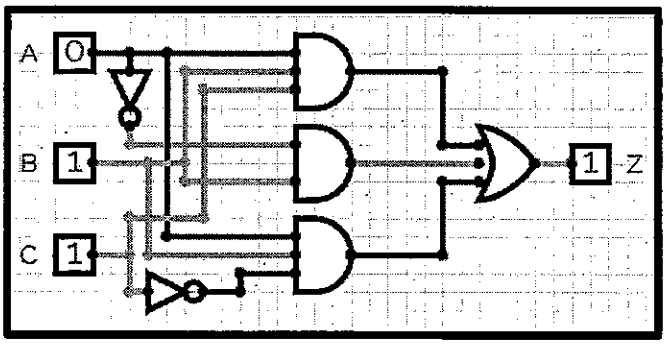
i. Binary
ii. Hexadecimal
iii. Decimal

Continued .....

c) Perform the subtraction 28_{10} -14_{10} by doing addition using their 8-bits signed 2's complement binary numbers and provide the final answer in decimal. Show all steps. [3 Marks]

QUESTION 2

a) Given circuit given below with the inputs A, B, and C, and the output Z. Answer the following questions.



i) Identify the output expression Z. [1 Mark]

Continued .....

ii) Simplify the Boolean expression for the output Z (from Question 2 (a) (i)) using Boolean Algebra. Show all steps. [3 Marks]

iii) Prove that the output of the Boolean Expression obtained before (from Question 2 (a) (i)) and after (from Question 2 (a) (ii)) simplification are the same using truth table. Show all steps.

[4 Marks]

Continued .....

b) Explain why the accuracy and precision are easier to maintain on digital systems as compared to analog systems. [2 Marks]

QUESTION 3

Design a synchronous counter that has three positive-edged triggered JK flip-flops and three inputs A, B and C. Design the counter based on the sequence listed below:

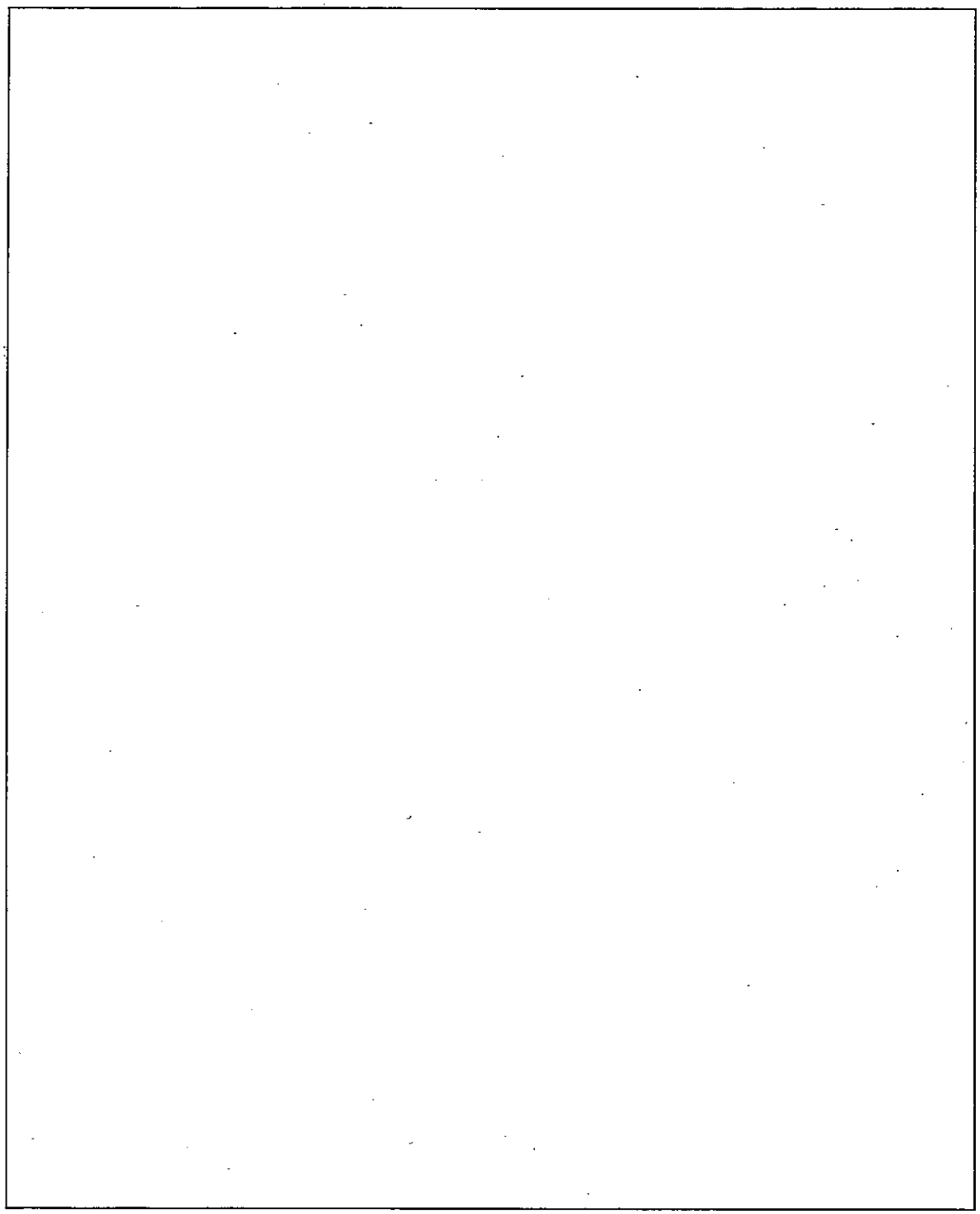
000, 010, 100, 110 and repeats.
Those undesired states go to Don't Care on the next clock pulse.

Your design should include:

i) State Transition Diagram by showing all possible states [1 Mark]

Continued .....

ii) By referring to JK flip flop Excitation Table, construct the Circuit Excitation Table. [4 Marks]



Continued .....

iii) Perform Karnaugh Map simplification for each of positive-edged triggered JK flip-flops inputs. [3 Marks]

iv) Draw the synchronous counter [2 Marks]

Continued .....

QUESTION 4

a) Design a combinational logic circuit with THREE inputs A, B, and C, and ONE output F. When the decimal equivalent binary input is **greater than 1, but less than 7**, the binary output is 1 otherwise the output is 0. The output of the first combination is Question 4 (a) (i). Perform the following steps.

i) Provide the truth table. [2 Marks]

A	B	C	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

ii) From the truth table, obtain the Boolean expression F in SOP form [1.5 Marks]

iii) Use K-map to simplify the Boolean expression obtained in Question 4 (a) (ii) [1.5 Marks]

		C'	C
A'	B'		
A'	B		
A	B		
A	B'		

Continued .....

iv) Draw the logic diagram for the simplified expression obtained in Question 4 (a) (iii) for the output F.

[1 Mark]

b) Perform the following arithmetic operations. Show all steps. [4 Marks]

i) $165_8 + 13_8$

ii) $165_8 - 13_8$

iii) $165_{16} + BA_{16}$

iv) $165_{16} - BA_{16}$

Continued .....

QUESTION 5

a) Explains the difference between synchronous and asynchronous counter. [1 Mark]

b) Draw a 2-bit asynchronous UP counter using positive-edge clocked JK flip-flop . [4 Mark]

c) Design a 4-bit Johnson counter by performing the following steps.

i) List out the 4-bit Johnson Sequence with the initial sequence of 0110.

[2 Marks]

Clock Pulse	Q0	Q1	Q2	Q3
0	0	1	1	0
1				
2				
3				
4				
5				
6				
7				

Continued .....

ii) Draw the 4-bit Johnson counter using D flop-flop. [3 Marks]

End of Page.